



DRV883x 低压 H 桥驱动器

1 特性

- H 桥电机驱动器
 - 驱动一个直流电机或其他负载
 - 低金属氧化物半导体场效应晶体管 (MOSFET) 导通电阻: 高侧 + 低侧 (HS + LS) 280mΩ
- 1.8A 最大驱动电流
- 独立的电机和逻辑电源引脚:
 - 电机 VM: 0 至 11V
 - 逻辑 VCC: 1.8 至 7V
- 脉宽调制 (PWM) 或 PH/EN 接口
 - DRV8837: 脉宽调制 (PWM), IN1/IN2
 - DRV8838: PH/EN
- 具有 120nA 最大睡眠电流的低功耗睡眠模式
 - nSLEEP 引脚
- 小型封装尺寸
 - 8 超薄小外形尺寸封装 (WSON) (PowerPAD™)
 - 2.0mm x 2.0mm
- 保护特性
 - VCC 欠压闭锁 (UVLO)
 - 过流保护 (OCP)
 - 热关断 (TSD)

2 应用范围

- 摄像机
- 数字单镜头反光 (DSLR) 镜头
- 消费类产品
- 玩具
- 机器人技术
- 医疗设备

3 说明

DRV883x 为摄像机、消费类产品、玩具和其它低电压或者电池供电的运动控制类应用提供了一个集成的电机驱动器解决方案。此器件能够驱动一个直流电机或其他诸如螺线管的器件。输出驱动器块由一个配置为 H 桥的 N 通道功率 MOSFET 组成, 以驱动电机绕组。一个内部电荷泵生成所需的栅极驱动电压。

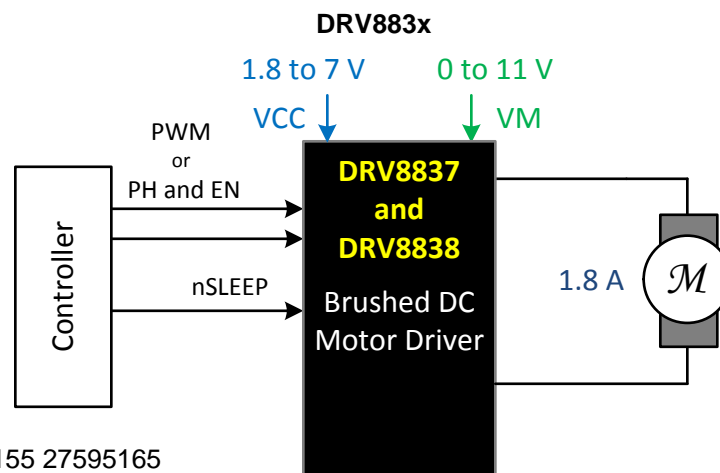
DRV883x 能够提供高达 1.8A 的输出电流。它运行在 0 至 11V 之间的电机电源电压, 以及 1.8V 至 7.0V 范围内的器件电源电压上。

DRV8837 具有一个 PWM (IN/IN) 输入接口; DRV8837 具有一个 PH/EN 输入接口 (此处应为 DRV8838 具有一个 PH/EN 输入接口)。这两个接口都与行业标准器件兼容。

还提供用于过流保护、短路保护、欠压闭锁和过热保护的内部关断功能。

器件信息

订货编号	封装	封装尺寸
DRV8837DSGR	WSON (8)	2.0mm x 2.0mm
DRV8838DSGR	WSON (8)	2.0mm x 2.0mm



TEL: +86-0755-27595155 27595165

FAX: +86-0755-27594792

WEB: [Http://www.ChipSourceTek.com](http://www.ChipSourceTek.com)

E-mail: Tony.Wang@ChipSourceTek.com InFo@ChipSourceTek.com





目录

1 特性.....	1	7.3 Feature Description.....	11
2 应用范围.....	1	7.4 Device Functional Modes.....	12
3 说明.....	1	8 Applications and Implementation	13
4 修订历史记录.....	2	8.1 Application Information.....	13
5 Terminal Configuration and Functions	3	8.2 Typical Applications.....	13
6 Specifications	4	9 Power Supply Recommendations	15
6.1 Absolute Maximum Ratings.....	4	10 Layout	16
6.2 Handling Ratings.....	4	10.1 Layout Guidelines.....	16
6.3 Recommended Operating Conditions.....	4	10.2 Layout Example.....	16
6.4 Thermal Information.....	4	11 Device and Documentation Support	17
6.5 Electrical Characteristics.....	5	11.1 Related Links.....	17
6.6 Timing Requirements.....	6	11.2 Trademarks.....	17
6.7 Typical Characteristics.....	8	11.3 Electrostatic Discharge Caution.....	17
7 Detailed Description	9	11.4 Glossary.....	17
7.1 Overview.....	9	12 机械封装和可订购信息	18
7.2 Functional Block Diagram.....	9		

4 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

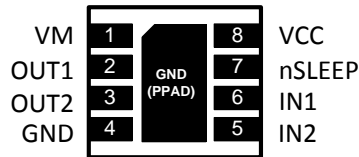
Changes from Revision B (December 2013) to Revision C	Page
• 已添加 DRV8838 器件信息、技术规格和时序图.....	1
• 已添加器件信息表.....	1
• 已添加一个 PWM 接口图.....	1
• Added more information to the Detailed Description and moved information from the Functional Description.....	9
• Added functional block diagram for DRV8838.....	10
• Added the Applications and Implementation section.....	13
• Added Power Supply Recommendations, Layout, Device and Documentation Support, and Packaging sections.....	15

Changes from Revision A (August 2012) to Revision B	Page
• 已更改 特性部分.....	1
• Changed Recommended Operating Conditions.....	4
• Changed Electrical Characteristics section.....	5
• Changed Timing Requirements section.....	6
• Changed Power Supplies and Input Pins section.....	11

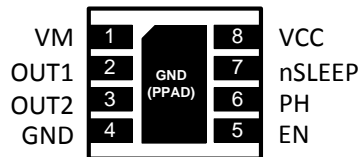


5 Terminal Configuration and Functions

DRV8837 DSG – WSON
(Top View)



DRV8838 DSG – WSON
(Top View)



Terminal Descriptions

TERMINAL		TYPE	DESCRIPTION
NAME	NUMBER		
POWER AND GROUND			
GND	4	PWR	Device ground Must be connected to ground
VCC	8	PWR	Logic Power supply Bypass to GND with a 0.1- μ F ceramic capacitor rated for VCC
VM	1	PWR	Motor power supply Bypass to GND with a 0.1- μ F ceramic capacitor rated for VM
CONTROL			
IN1/PH	6	I	IN1 or PHASE input See Detailed Description for more information
IN2/EN	5	I	IN2 or ENABLE input
nSLEEP	7	I	Sleep mode input Logic low puts the device in low-power sleep mode; logic high for normal operation; internal pulldown resistor
OUTPUT			
OUT1	2	O	Motor output
OUT2	3	O	Connect to motor winding



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

	MIN	MAX	UNIT
Motor power supply voltage range (VM)	-0.3	12	V
Logic power supply voltage range (VCC)	-0.3	7	V
Control pin voltage range (IN1, IN2, PH, EN, nSLEEP)	-0.5	7	V
Peak drive current (OUT1, OUT2)	Internally limited		A
T _J , operating virtual junction temperature range	-40	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

6.2 Handling Ratings

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
T _{stg} Storage temperature range	-60	150	°C

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
VM Motor power supply voltage range	0	11	V
VCC Logic power supply voltage range	1.8	7	V
I _{OUT} Motor peak current	0	1.8	A
f _{PWM} Externally applied PWM frequency	0	250	kHz
V _{LOGIC} Logic level input voltage	0	5.5	V
T _A Operating ambient temperature	-40	85	°C

- (1) Power dissipation and thermal limits must be observed.

6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC ⁽¹⁾	DRV8837, DRV8838	UNIT
	WSO8 (8 TERMINALS)	
θ _{JA} Junction-to-ambient thermal resistance ⁽²⁾	60.9	°C/W
θ _{JC(TOP)} Junction-to-case (top) thermal resistance ⁽³⁾	71.4	
θ _{JB} Junction-to-board thermal resistance ⁽⁴⁾	32.2	
ψ _{JT} Junction-to-top characterization parameter ⁽⁵⁾	1.6	
ψ _{JB} Junction-to-board characterization parameter ⁽⁶⁾	32.8	
θ _{JC(BOTTOM)} Junction-to-case (bottom) thermal resistance ⁽⁷⁾	9.8	

- (1) For more information about traditional and new thermal limits, see the IC Package Thermal Metrics Report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.



6.5 Electrical Characteristics

T_A = 25°C, over recommended operating conditions unless otherwise noted

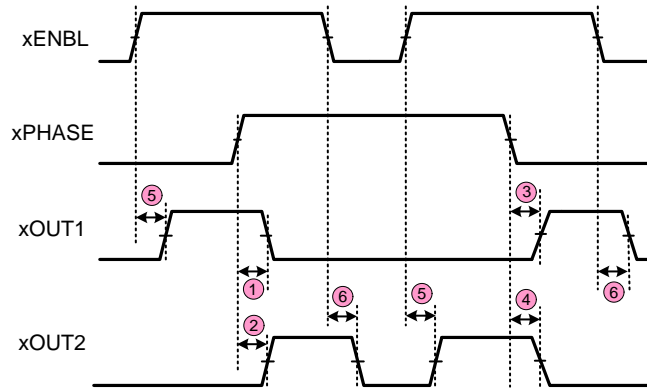
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, VCC)						
VM	VM operating voltage		0		11	V
I _{VM}	VM operating supply current	VM = 5 V; VCC = 3 V; No PWM		40	100	μA
		VM = 5 V; VCC = 3 V; 50 kHz PWM		0.8	1.5	mA
I _{VMQ}	VM sleep mode supply current	VM = 5 V; VCC = 3 V; nSLEEP = 0		30	95	nA
VCC	VCC operating voltage		1.8		7	V
I _{VCC}	VCC operating supply current	VM = 5 V; VCC = 3 V; No PWM		300	500	μA
		VM = 5 V; VCC = 3 V; 50 kHz PWM		0.7	1.5	mA
I _{VCCQ}	VCC sleep mode supply current	VM = 5 V; VCC = 3 V; nSLEEP = 0		5	25	nA
CONTROL INPUTS (IN1/PH, IN2/EN, nSLEEP)						
V _{IL}	Input logic low voltage		0.25 × VCC	0.38 × VCC		V
V _{IH}	Input logic high voltage			0.46 × VCC	0.5 × VCC	V
V _{HYS}	Input logic hysteresis			0.08 × VCC		mV
I _{IL}	Input logic low current	V _{IN} = 0 V	-5		5	μA
I _{IH}	Input logic high current	V _{IN} = 3.3 V			50	μA
		V _{IN} = 3.3 V, DRV8838 nSLEEP pin		60		μA
R _{PD}	Pulldown resistance			100		kΩ
		DRV8838 nSLEEP pin		55		kΩ
MOTOR DRIVER OUTPUTS (OUT1, OUT2)						
R _{DS(ON)}	HS + LS FET on-resistance	VM = 5 V; VCC = 3 V; I _O = 800 mA; T _J = 25°C		280	330	mΩ
I _{OFF}	Off-state leakage current	V _{OUT} = 0 V	-200		200	nA
PROTECTION CIRCUITS						
V _{UVLO}	VCC undervoltage lockout	VCC falling			1.7	V
		VCC rising			1.8	V
I _{OCP}	Overcurrent protection trip level		1.9		3.5	A
t _{DEG}	Overcurrent deglitch time			1		μs
t _{RETRY}	Overcurrent retry time			1		ms
T _{TSD}	Thermal shutdown temperature	Die temperature T _J	150	160	180	°C



6.6 Timing Requirements

T_A = 25°C, V_M = 5 V, V_{CC} = 3 V, R_L = 20 Ω

NUMBER	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
1	t ₁	Delay time, PHASE high to OUT1 low		160	ns
2	t ₂	Delay time, PHASE high to OUT2 high		200	ns
3	t ₃	Delay time, PHASE low to OUT1 high		200	ns
4	t ₄	Delay time, PHASE low to OUT2 low		160	ns
5	t ₅	Delay time, ENBL high to OUTx high		200	ns
6	t ₆	Delay time, ENBL low to OUTx low		160	ns
7	t ₇	Output enable time		300	ns
8	t ₈	Output disable time		300	ns
9	t ₉	Delay time, INx high to OUTx high		160	ns
10	t ₁₀	Delay time, INx low to OUTx low		160	ns
11	t ₁₁	Output rise time	30	188	ns
12	t ₁₂	Output fall time	30	188	ns
	t _{wake}	Wake time, nSLEEP rising edge to part active		30	μs



DRV8838

Figure 1. Input and Output Timing for DRV8838

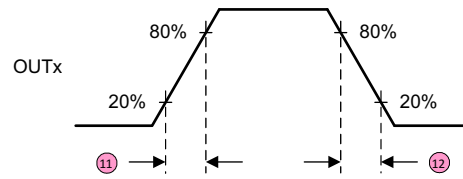
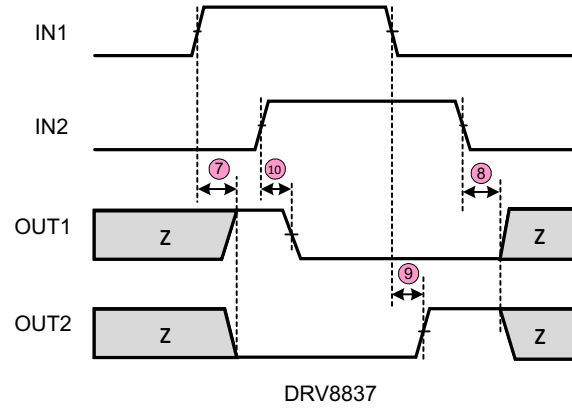
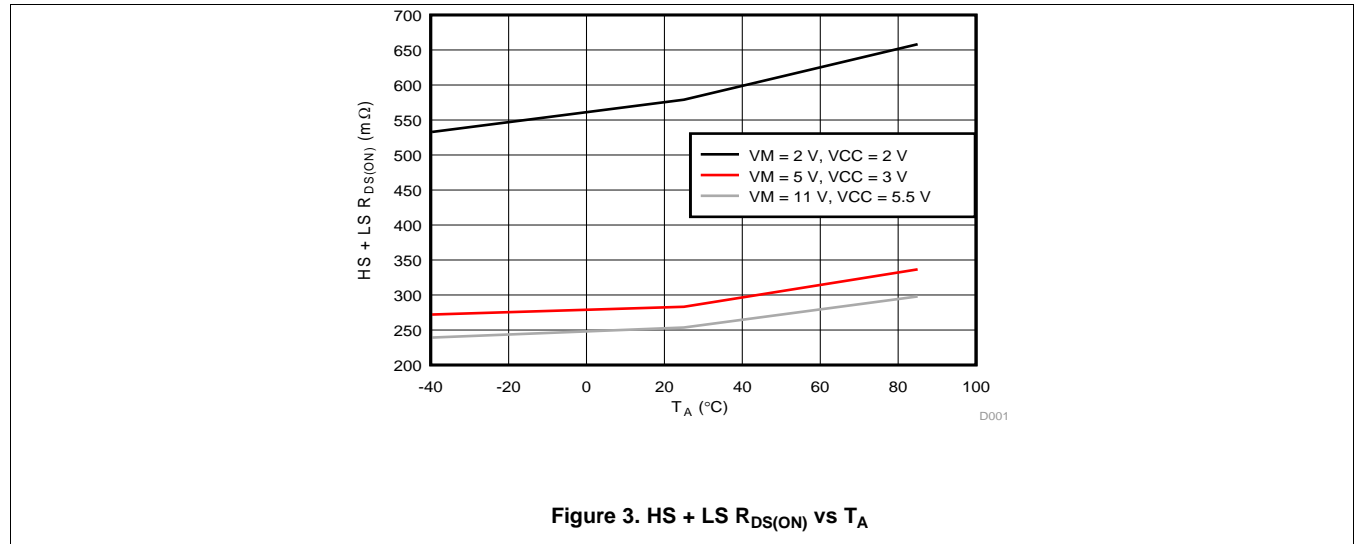


Figure 2. Input and Output Timing for DRV8837



6.7 Typical Characteristics

Plot generated using characterization data





7 Detailed Description

7.1 Overview

The DRV883x is a H-bridge driver that can drive one DC motor or other devices like solenoids. The outputs are controlled using either a PWM interface (IN1/IN2) on the DRV8837 or a PH/EN interface on the DRV8838.

A low-power sleep mode is included, which can be enabled using the nSLEEP pin.

These devices greatly reduce the component count of motor driver systems by integrating the necessary driver FETs and FET control circuitry into a single device. In addition, the DRV883x adds protection features above traditional discrete implementations: undervoltage lockout, overcurrent protection, and thermal shutdown.

7.2 Functional Block Diagram

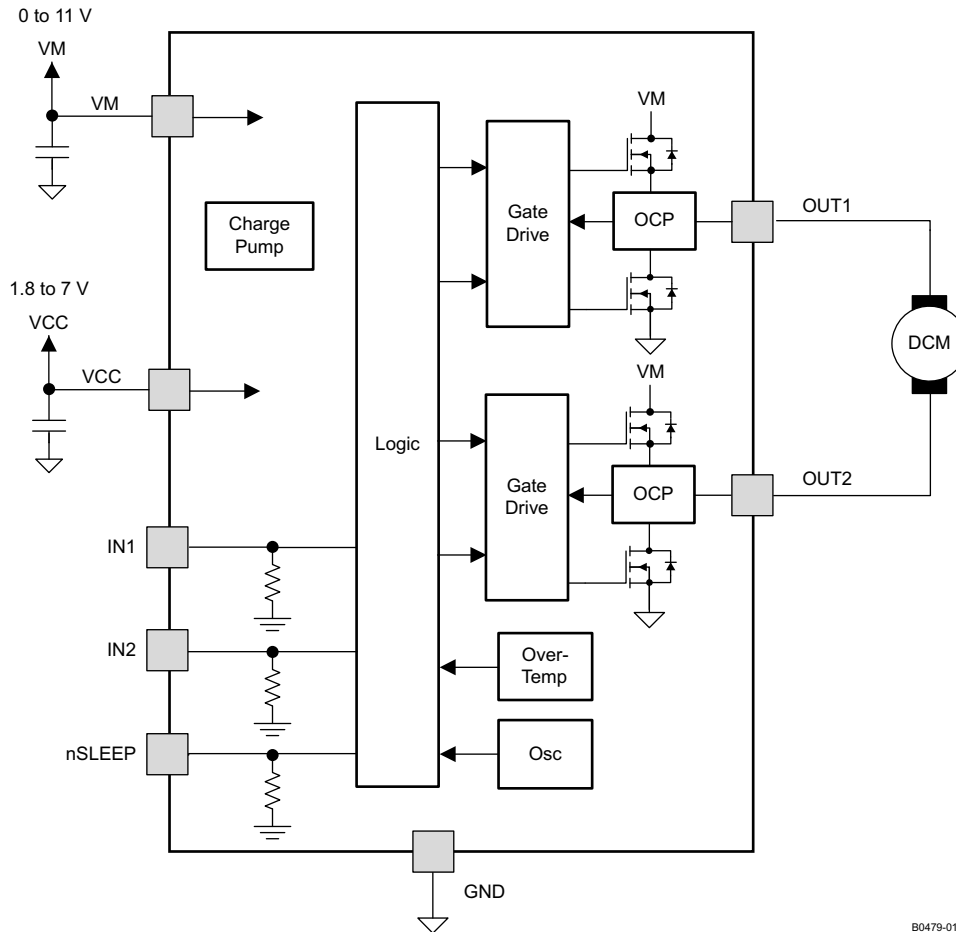


Figure 4. DRV8837 Functional Block Diagram

B0479-01



Functional Block Diagram (continued)

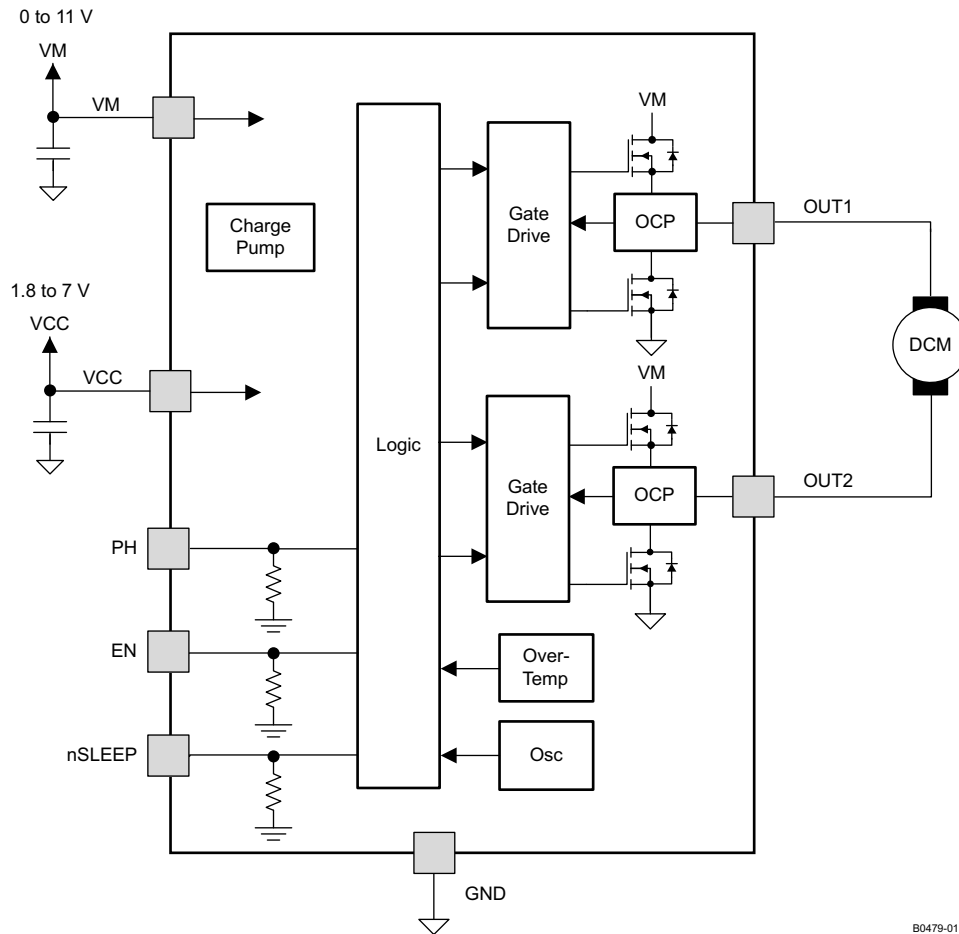


Figure 5. DRV8838 Functional Block Diagram

B0479-01



7.3 Feature Description

7.3.1 Bridge Control

The DRV8837 is controlled using a PWM input interface, also called an IN/IN interface. Each output is controlled by a corresponding input pin.

Table 1 shows the logic for the DRV8837 device:

Table 1. DRV8837 Device Logic

nSLEEP	IN1	IN2	OUT1	OUT2	Function (DC Motor)
0	X	X	Z	Z	Coast
1	0	0	Z	Z	Coast
1	0	1	L	H	Reverse
1	1	0	H	L	Forward
1	1	1	L	L	Brake

The DRV8838 is controlled using a PHASE/ENABLE interface. This interface uses one pin to control the H-bridge current direction, and one pin to enable or disable the H-bridge.

Table 2 shows the logic for the DRV8838:

Table 2. DRV8838 Device Logic

nSLEEP	PH	EN	OUT1	OUT2	Function (DC Motor)
0	X	X	Z	Z	Coast
1	X	0	L	L	Brake
1	1	1	L	H	Reverse
1	0	1	H	L	Forward

7.3.2 Sleep Mode

If the nSLEEP pin is brought to a logic-low state, the DRV883x enters a low-power sleep mode. In this state, all unnecessary internal circuitry is powered down.

7.3.3 Power Supplies and Input Terminals

The input pins may be driven within their recommended operating conditions with or without the VCC and/or VM power supplies present. No leakage current path will exist to the supply. There is a weak pulldown resistor (approximately 100 kΩ) to ground on each input pin.

VCC and VM may be applied and removed in any order. When VCC is removed, the device will enter a low power state and draw very little current from VM. VCC and VM may be connected together if the supply voltage is between 1.8 and 7 V.

The VM voltage supply does not have any undervoltage lockout protection (UVLO), so as long as VCC > 1.8 V; the internal device logic will remain active. This means that the VM pin voltage may drop to 0 V, however, the load may not be sufficiently driven at low VM voltages.

7.3.4 Protection Circuits

The DRV883x is fully protected against VCC undervoltage, overcurrent, and overtemperature events.

VCC Undervoltage Lockout: If at any time the voltage on the VCC pin falls below the undervoltage lockout threshold voltage, all FETs in the H-bridge will be disabled. Operation resumes when VCC rises above the UVLO threshold.

Overcurrent Protection (OCP): An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than tDEG, all FETs in the H-bridge will be disabled. Operation resumes automatically after t_{RETRY} has elapsed. Overcurrent conditions will be detected on both the high-side and low-side devices. A short to VM, GND, or from OUT1 to OUT2 results in an overcurrent condition



Thermal Shutdown (TSD): If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled. After the die temperature falls to a safe level, operation automatically resumes.

Table 3. Fault Behavior

Fault	Condition	H-bridge	Recovery
VCC undervoltage (UVLO)	$VCC < 1.7\text{ V}$	Disabled	$VCC > 1.8\text{ V}$
Overcurrent (OCP)	$I_{OUT} > 1.9\text{ A (MIN)}$	Disabled	t_{RETRY} elapses
Thermal Shutdown (TSD)	$T_J > 150^\circ\text{C (MIN)}$	Disabled	$T_J < 150^\circ\text{C}$

7.4 Device Functional Modes

The DRV883x is active unless the nSLEEP pin is brought logic low. In sleep mode the H-bridge FETs are disabled Hi-Z. The DRV883x is brought out of sleep mode automatically if nSLEEP is brought logic high.

The H-bridge outputs are disabled during undervoltage lockout, overcurrent, and overtemperature fault conditions.

Table 4. Operation Modes

Mode	Condition	H-bridge
Operating	nSLEEP pin = 1	Operating
Sleep mode	nSLEEP pin = 0	Disabled
Fault encountered	Any fault condition met	Disabled



8 Applications and Implementation

8.1 Application Information

The DRV883x device is used to drive one DC motor or other devices like solenoids. The following design procedure can be used to configure the DRV883x.

8.2 Typical Applications

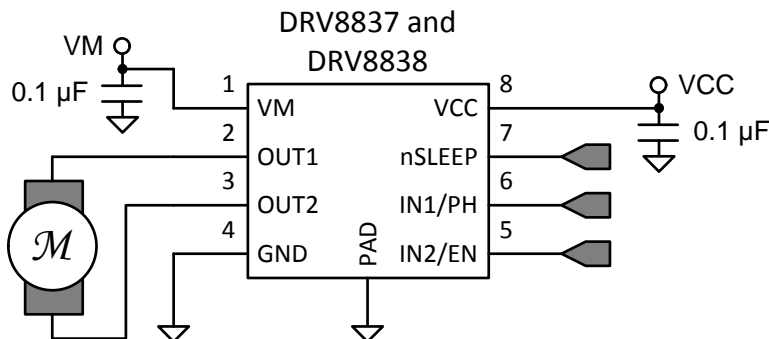


Figure 6. Schematic of DRV883x Application

8.2.1 Design Requirements

Table 5 shows required parameters for a typical usage case.

Table 5. System Design Requirements

Design Parameter	Reference	Example Value
Motor supply voltage	VM	9 V
Logic supply voltage	VCC	3.3 V
Target RMS current	I _{OUT}	0.8 A

8.2.2 Detailed Design Procedure

8.2.2.1 Power Dissipation

Power dissipation in the DRV883x is dominated by the power dissipated in the output FET resistance, or R_{DS(ON)}. Average power dissipation when running a stepper motor can be roughly estimated by:

$$P_{TOT} = R_{DS(ON)} \times (I_{OUT(RMS)})^2$$

where

- P_{TOT} is the total power dissipation
- R_{DS(ON)} is the resistance of the HS plus LS FETs
- I_{OUT(RMS)} is the RMS or DC output current being supplied to the load

(1)

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that R_{DS(ON)} increases with temperature, so as the device heats, the power dissipation increases.

The DRV883x has thermal shutdown protection. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.



8.2.3 Application Performance Plots

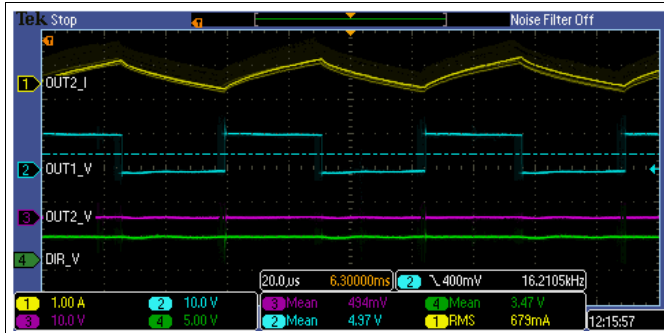


Figure 7. 50% Duty Cycle, Forward Direction



Figure 8. 50% Duty Cycle, Reverse Direction

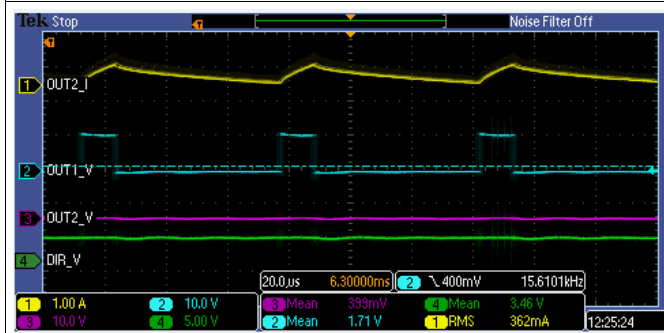


Figure 9. 20% Duty Cycle, Forward Direction



Figure 10. 20% Duty Cycle, Reverse Direction



9 Power Supply Recommendations

VCC and VM may be applied and removed in any order. When VCC is removed, the device enters a low power state and draws very little current from VM. VCC and VM may be connected together if the supply voltage is between 1.8 and 7 V.

Bypass VM and VCC with 0.1- μ F ceramic capacitors rated for VM and VCC. Place these capacitors as close to the device as possible.

The VM voltage supply does not have any undervoltage lockout protection, so as long as $VCC > 1.8$ V; the internal device logic will remain active. This means that the VM pin voltage may drop to 0 V; however, the load may not be sufficiently driven at low VM voltages.



10 Layout

10.1 Layout Guidelines

The VM and VCC terminals should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1 μF rated for VM and VCC. These capacitors should be placed as close to the VM and VCC pins as possible with a thick trace or ground plane connection to the device GND pin.

10.2 Layout Example

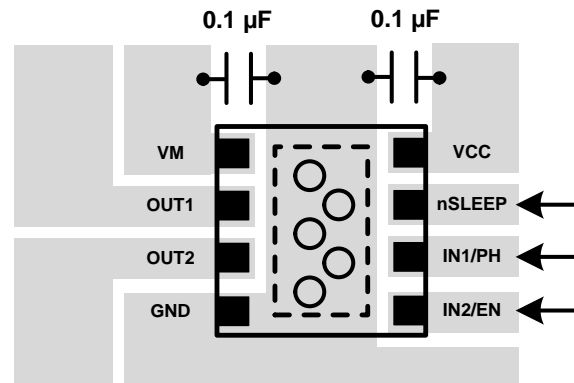


Figure 11. Simplified Layout Example



11 Device and Documentation Support

11.1 Related Links

The following table lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 6. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DRV8837	Click here	Click here	Click here	Click here	Click here
DRV8838	Click here	Click here	Click here	Click here	Click here

11.2 Trademarks

PowerPAD is a trademark of Texas Instruments.

11.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.



12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 要获得这份数据表的浏览器版本，请查阅左侧导航栏。



重要声明

德州仪器(TI)及其下属子公司有权根据 JESD46 最新标准,对所提供的产品和服务进行更正、修改、增强、改进或其它更改,并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息,并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内,且 TI 认为有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定,否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应用相关的风险,客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息,不能构成从 TI 获得使用这些产品或服务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可,或是 TI 的专利权或其它知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分,仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时,如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分,则会失去相关 TI 组件或服务的所有明示或暗示授权,且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意,尽管任何应用相关信息或支持仍可能由 TI 提供,但他们将独立负责满足与其产品及其在应用中使用的 TI 产品相关的所有法律、法规和安全相关要求。客户声明并同意,他们具备制定与实施安全措施所需的全部专业技术和知识,可预见故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中,为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此,此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III (或类似的生命攸关医疗设备)的授权许可,除非各方授权官员已经达成了专门管控此类使用的特别协议。

只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同意,对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用,其风险由客户单独承担,并且由客户独立负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品,这些产品主要用于汽车。在任何情况下,因使用非指定产品而无法达到 ISO/TS16949 要求, TI 不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com.cn/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com.cn/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址: 上海市浦东新区世纪大道1568号, 中建大厦32楼邮政编码: 200122
Copyright © 2014, 德州仪器半导体技术(上海)有限公司

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8837DSGR	ACTIVE	WSO	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	837	Samples
DRV8837DSGT	ACTIVE	WSO	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	837	Samples
DRV8838DSGR	ACTIVE	WSO	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU Call TI	Level-2-260C-1 YEAR	-40 to 85	838	Samples
DRV8838DSGT	ACTIVE	WSO	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	838	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8837DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
DRV8837DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
DRV8838DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

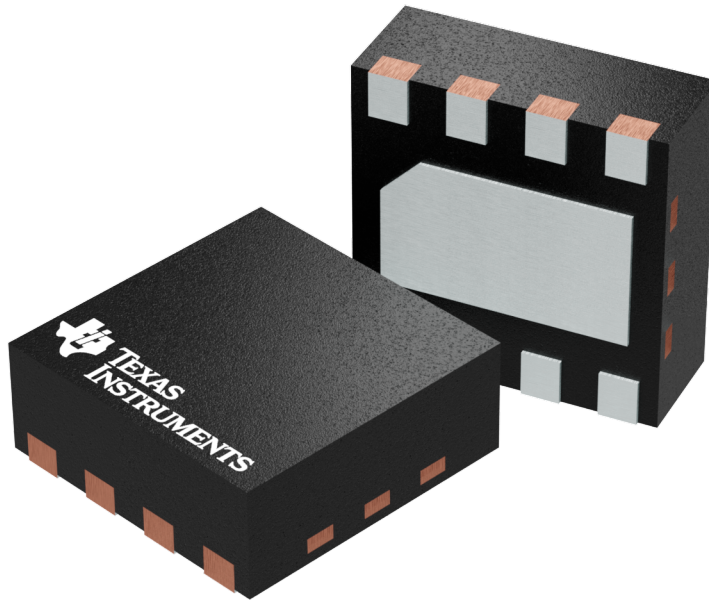
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8837DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
DRV8837DSGT	WSON	DSG	8	250	210.0	185.0	35.0
DRV8838DSGT	WSON	DSG	8	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DSG 8

WSON - 0.8 mm max height

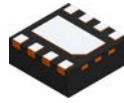
PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4208210/C

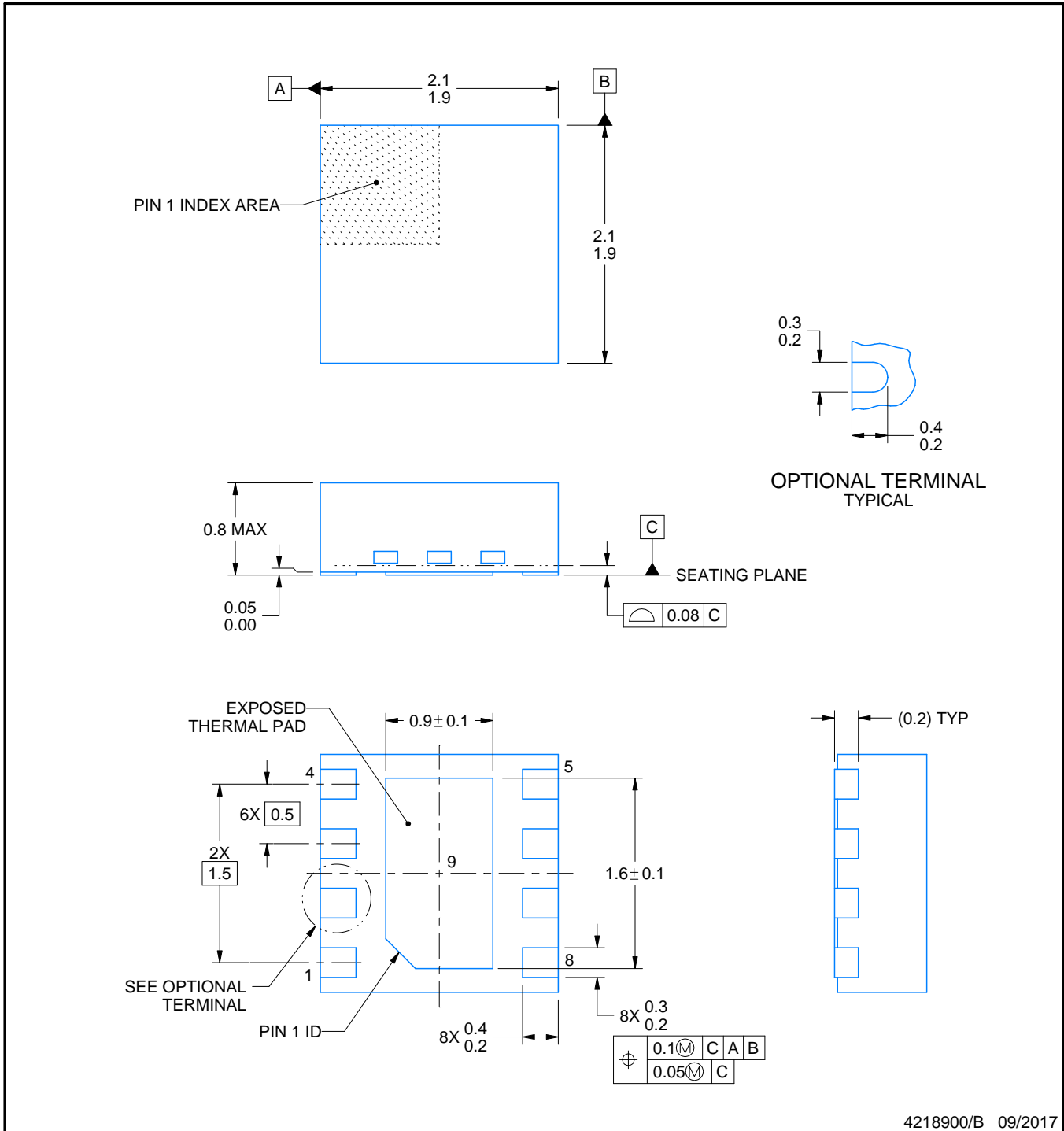
DSG0008A



PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4218900/B 09/2017

NOTES:

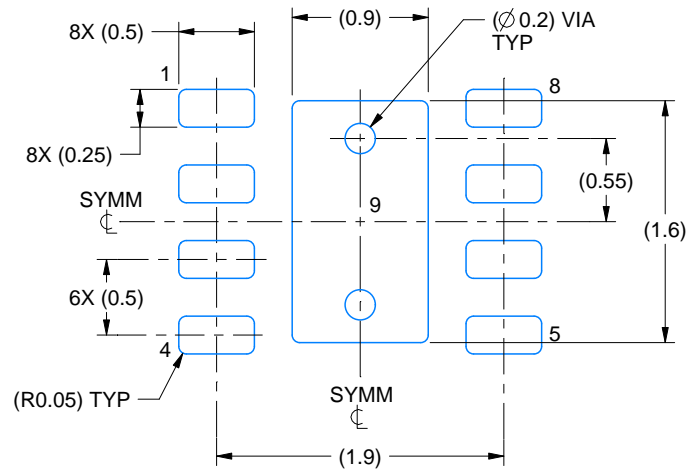
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

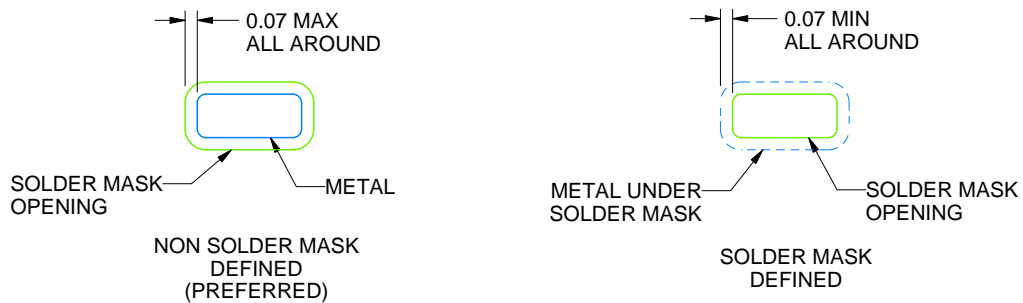
DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218900/B 09/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

重要声明

德州仪器 (TI) 公司有权按照最新发布的 JESD46 对其半导体产品和服务进行纠正、增强、改进和其他修改，并不再按最新发布的 JESD48 提供任何产品和服务。买方在下订单前应获取最新的相关信息，并验证这些信息是否完整且是最新的。

TI 公布的半导体产品销售条款 (<http://www.ti.com/sc/docs/stdterms.htm>) 适用于 TI 已认证和批准上市的已封装集成电路产品的销售。另有其他条款可能适用于其他类型 TI 产品及服务的使用或销售。

复制 TI 数据表上 TI 信息的重要部分时，不得变更该等信息，且必须随附所有相关保证、条件、限制和通知，否则不得复制。TI 对该等复制文件不承担任何责任。第三方信息可能受到其它限制条件的制约。在转售 TI 产品或服务时，如果存在对产品或服务参数的虚假陈述，则会失去相关 TI 产品或服务的明示或暗示保证，且构成不公平的、欺诈性商业行为。TI 对此类虚假陈述不承担任何责任。

买方和在系统中整合 TI 产品的其他开发人员（总称“设计人员”）理解并同意，设计人员在设计应用时应自行实施独立的分析、评价和判断，且应全权负责并确保应用的安全性，及设计人员的应用（包括应用中使用的 TI 产品）应符合所有适用的法律法规及其他相关要求。设计人员就自己设计的应用声明，其具备制订和实施下列保障措施所需的一切必要专业知识，能够 (1) 预见故障的危险后果，(2) 监视故障及其后果，以及 (3) 降低可能导致危险的故障几率并采取适当措施。设计人员同意，在使用或分发包含 TI 产品的任何应用前，将彻底测试该等应用和和该等应用所用 TI 产品的功能而设计。

TI 提供技术、应用或其他设计建议、质量特点、可靠性数据或其他服务或信息，包括但不限于与评估模块有关的参考设计和材料（总称“TI 资源”），旨在帮助设计人员开发整合了 TI 产品的应用，如果设计人员（个人，或如果是代表公司，则为设计人员的公司）以任何方式下载、访问或使用任何特定的 TI 资源，即表示其同意仅为该等目标，按照本通知的条款使用任何特定 TI 资源。

TI 所提供的 TI 资源，并未扩大或以其他方式修改 TI 对 TI 产品的公开适用的质保及质保免责声明；也未导致 TI 承担任何额外的义务或责任。TI 有权对其 TI 资源进行纠正、增强、改进和其他修改。除特定 TI 资源的公开文档中明确列出的测试外，TI 未进行任何其他测试。

设计人员只有在开发包含该等 TI 资源所列 TI 产品的应用时，才被授权使用、复制和修改任何相关单项 TI 资源。但并未依据禁止反言原则或其他法律授予您任何 TI 知识产权的任何其他明示或默示的许可，也未授予您 TI 或第三方的任何技术或知识产权的许可，该等许可包括但不限于任何专利权、版权、屏蔽作品权或与应用 TI 产品或服务的任何整合、机器制作、流程相关的其他知识产权。涉及或参考了第三方产品或服务的信息不构成使用此类产品或服务的许可或与其相关的保证或认可。使用 TI 资源可能需要您向第三方获得对该等第三方专利或其他知识产权的许可。

TI 资源系“按原样”提供。TI 兹免除对资源及其使用作出所有其他明确或默示的保证或陈述，包括但不限于对准确性或完整性、产权保证、无屡发故障保证，以及适销性、适合特定用途和不侵犯任何第三方知识产权的任何默认保证。TI 不负任何责任，包括但不限于因组合产品所致或与之有关的申索，也不为或对设计人员进行辩护或赔偿，即使该等产品组合已列于 TI 资源或其他地方。对因 TI 资源或其使用引起或与之有关的任何实际的、直接的、特殊的、附带的、间接的、惩罚性的、偶发的、从属或惩戒性损害赔偿，不管 TI 是否获悉可能会产生上述损害赔偿，TI 概不负责。

除 TI 已明确指出特定产品已达到特定行业标准（例如 ISO/TS 16949 和 ISO 26262）的要求外，TI 不对未达到任何该等行业标准要求而承担任何责任。

如果 TI 明确宣称产品有助于功能安全或符合行业功能安全标准，则该等产品旨在帮助客户设计和创作自己的符合相关功能安全标准和要求的的应用。在应用内使用产品的行为本身不会配有 任何安全特性。设计人员必须确保遵守适用于其应用的相关安全要求和标准而设计。设计人员不可将任何 TI 产品用于关乎性命的医疗设备，除非已由各方获得授权的管理人员签署专门的合同对此类应用专门作出规定。关乎性命的医疗设备是指出现故障会导致严重身体伤害或死亡的医疗设备（例如生命保障设备、心脏起搏器、心脏除颤器、人工心脏泵、神经刺激器以及植入设备）。此类设备包括但不限于，美国食品药品监督管理局认定为 III 类设备的设备，以及在美国以外的其他国家或地区认定为同等类别设备的所有医疗设备。

TI 可能明确指定某些产品具备某些特定资格（例如 Q100、军用级或增强型产品）。设计人员同意，其具备一切必要专业知识，可以为自己的应用选择适合的产品，并且正确选择产品的风险由设计人员承担。设计人员单方面负责遵守与该等选择有关的所有法律或监管要求。

设计人员同意向 TI 及其代表全额赔偿因其不遵守本通知条款和条件而引起的任何损害、费用、损失和/或责任。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2018 德州仪器半导体技术（上海）有限公司