Features

- Multi-Band operation 400 to 5000MHz
- MIPI RFFE V2.1 interface compatible
- Compact 2.0mm x 2.0mm QFN-16 package, MSL1

Applications

- 2G/3G/4G System

Description

The FM1024 V1.0 is a CMOS, high isolation, Silicon-On-Insulator (SOI) dual-pole, four -throw (DP4T) switch. The switch provides high linearity, low insertion loss and high isolation performances.

The FM1024 V1.0 is compatible with MIPI RFFE V2.1 interface, which is a key requirement for many cellular transceivers. RFOUT1, RFOUT2 pins are connected to one of the four other RFIN port pins (RFIN1/RFIN2/RFIN3/RFIN4) through a low insertion loss path, while maintaining a very high isolation path to the other ports. No external DC blocking capacitors are required on the RF path as long as no DC voltage is applied externally.

The FM1024 V1.0 is provided in a QFN (16-pin, 2.0 x 2.0) package. A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 1, too. Signal pin assignments and functional pin descriptions are provided in Table 1.

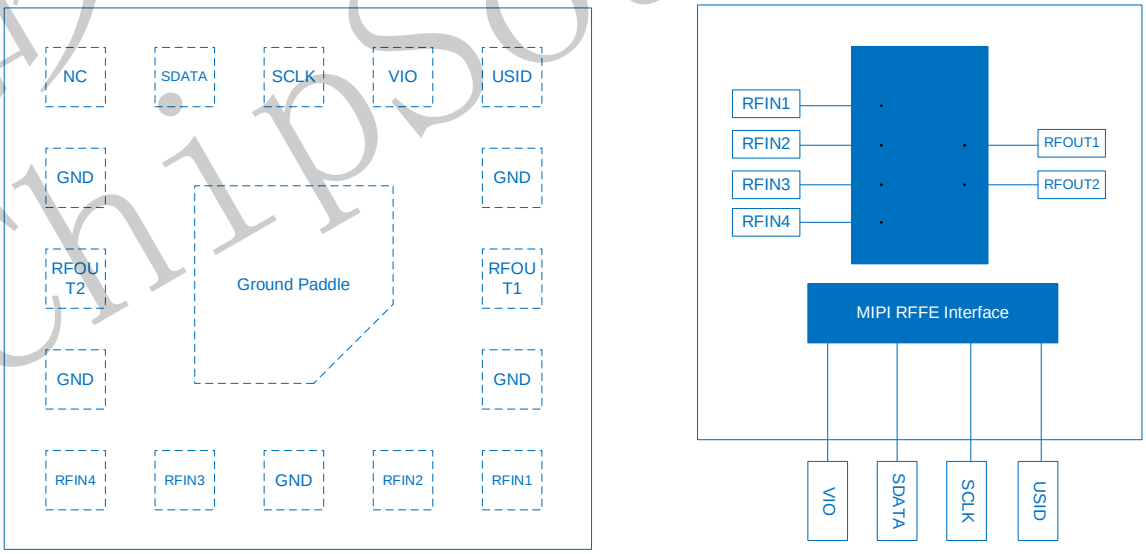


Figure 1 Functional Block Diagram and Pin Configuration

Function Characteristics

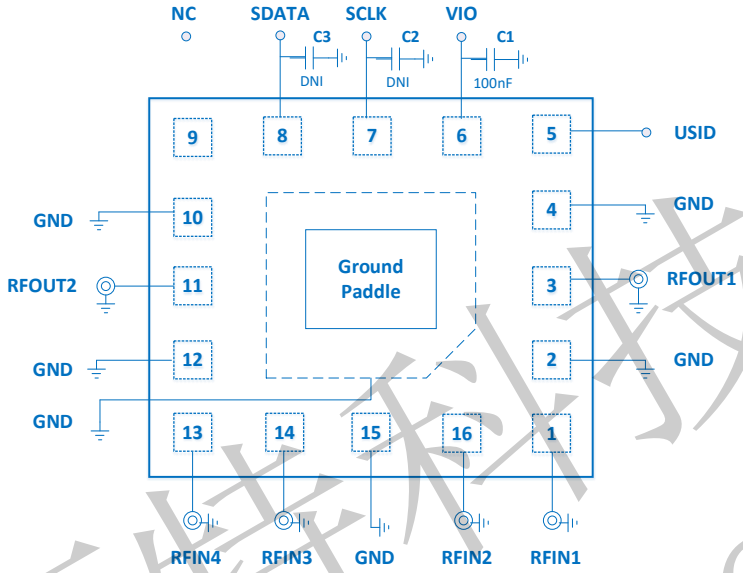


Figure 2 Application Circuit

Table 1 Pin Descriptions

NO.	Name	Description	NO.	Name	Description
1	RFIN1	RF Input Port1	9	NC	Not Connected (can be grounded)
2	GND	Ground	10	GND	Ground
3	RFOUT1	RF Output Port1	11	RFOUT2	RF Output Port2
4	GND	Ground	12	GND	Ground
5	USID	USID Select Pin	13	RFIN4	RF Input Port4
6	VIO	Supply Voltage	14	RFIN3	RF Input Port3
7	SCLK	RFFE Clock Bus	15	GND	GND
8	SDATA	RFFE Data Bus	16	RFIN2	RF Input Port2
Ground Paddle	GND	Ground			

Table 2 Register Mapping for RF Operating Modes

Register1	Output Switching Control Register							
Patch	D7	D6	D5	D4	D3	D2	D1	D0
DPDT Direct DP4T Direct (Default)	x	x	x	x	x	x	x	0
DP4T Cross	x	x	x	x	x	x	x	1

DP4T Combined Working State, Register1[0]=0

State	Mode (Register1[0]=0)		Register0 (DP4T switching Control Register)							
			D7	D6	D5	D4	D3	D2	D1	D0
1	Isolation mode	Isolation mode	x	x	0	0	0	0	0	0
2	Input1 -> Output1; Output2 Isolation	Single through mode	x	x	0	0	0	0	0	1
3	Input1 -> Output1; Input2 -> Output2	Dual through mode	x	x	0	1	0	0	1	1
4	Input1 -> Output1; Input3 -> Output2	Dual through mode	x	x	0	1	0	1	0	1
5	Input1 -> Output1; Input4 -> Output2	Dual through mode	x	x	0	1	1	0	0	1
6	Input2 -> Output1; Output2 Isolation	Single through mode	x	x	0	0	0	0	1	0
7	Input2 -> Output1; Input1 -> Output2	Dual through mode	x	x	1	0	0	0	1	1
8	Input2 -> Output1; Input3 -> Output2	Dual through mode	x	x	0	1	0	1	1	0
9	Input2 -> Output1; Input4 -> Output2	Dual through mode	x	x	0	1	1	0	1	0
10	Input3 -> Output1; Output2 Isolation	Single through mode	x	x	0	0	0	1	0	0
11	Input3 -> Output1; Input1 -> Output2	Dual through mode	x	x	1	0	0	1	0	1
12	Input3 -> Output1; Input2 -> Output2	Dual through mode	x	x	1	0	0	1	1	0
13	Input3 -> Output1; Input4 -> Output2	Dual through mode	x	x	0	1	1	1	0	0
14	Input4 -> Output1; Output2 Isolation	Single through mode	x	x	0	0	1	0	0	0
15	Input4 -> Output1; Input1 -> Output2	Dual through mode	x	x	1	0	1	0	0	1
16	Input4 -> Output1; Input2 -> Output2	Dual through mode	x	x	1	0	1	0	1	0
17	Input4 -> Output1; Input3 -> Output2	Dual through mode	x	x	1	0	1	1	0	0
18	Input1 -> Output2; Output1 Isolation	Single through mode	x	x	1	1	0	0	0	1
19	Input2 -> Output2; Output1 Isolation	Single through mode	x	x	1	1	0	0	1	0
20	Input3 -> Output2; Output1 Isolation	Single through mode	x	x	1	1	0	1	0	0
21	Input4 -> Output2; Output1 Isolation	Single through mode	x	x	1	1	1	0	0	0

DP4T Combined Working State, Register1[0]=1

State	Mode (Register1[0]=1)		Register0 (DP4T switching Control Register)							
			D7	D6	D5	D4	D3	D2	D1	D0
1	Isolation mode	Isolation mode	x	x	0	0	0	0	0	0
2	Input1 -> Output2; Output1 Isolation	Single through mode	x	x	0	0	0	0	0	1
3	Input1 -> Output2; Input2 -> Output1	Dual through mode	x	x	0	1	0	0	1	1
4	Input1 -> Output2; Input3 -> Output1	Dual through mode	x	x	0	1	0	1	0	1
5	Input1 -> Output2; Input4 -> Output1	Dual through mode	x	x	0	1	1	0	0	1
6	Input2 -> Output2; Output1 Isolation	Single through mode	x	x	0	0	0	0	1	0
7	Input2 -> Output2; Input1 -> Output1	Dual through mode	x	x	1	0	0	0	1	1
8	Input2 -> Output2; Input3 -> Output1	Dual through mode	x	x	0	1	0	1	1	0
9	Input2 -> Output2; Input4 -> Output1	Dual through mode	x	x	0	1	1	0	1	0
10	Input3 -> Output2; Output1 Isolation	Single through mode	x	x	0	0	0	1	0	0
11	Input3 -> Output2; Input1 -> Output1	Dual through mode	x	x	1	0	0	1	0	1
12	Input3 -> Output2; Input2 -> Output1	Dual through mode	x	x	1	0	0	1	1	0
13	Input3 -> Output2; Input4 -> Output1	Dual through mode	x	x	0	1	1	1	0	0
14	Input4 -> Output2; Output1 Isolation	Single through mode	x	x	0	0	1	0	0	0
15	Input4 -> Output2; Input1 -> Output1	Dual through mode	x	x	1	0	1	0	0	1
16	Input4 -> Output2; Input2 -> Output1	Dual through mode	x	x	1	0	1	0	1	0
17	Input4 -> Output2; Input3 -> Output1	Dual through mode	x	x	1	0	1	1	0	0
18	Input1 -> Output1; Output2 Isolation	Single through mode	x	x	1	1	0	0	0	1
19	Input2 -> Output1; Output2 Isolation	Single through mode	x	x	1	1	0	0	1	0
20	Input3 -> Output1; Output2 Isolation	Single through mode	x	x	1	1	0	1	0	0
21	Input4 -> Output1; Output2 Isolation	Single through mode	x	x	1	1	1	0	0	0

Notice

x—Either 0 or 1

Electrical Characteristics

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Condition
Supply Voltage	V_{IO}	-0.3	2.5	V	T_A=25℃
RFFE Bus Voltage (SDATA, SCLK)	V_I	-0.3	2.5	V	T_A=25℃
RFFE USID Voltage	V_{USID}	-0.3	2.5	V	T_A=25℃
Max RF Input Power (RFIN1/2/3/4 to RFOUT1/2)	P_{INMAX}		37	dBm	F_0=0.4 to 3.8GHz, 20% DC V_{IO}=1.8V, VSWR=1:1, TA=25℃
			36	dBm	F_0=4.0 to 5.8GHz, 20% DC V_{IO}=1.8V, VSWR=1:1, TA=25℃
Device Operating Temperature	T_{OP}	-40	90	℃	
Device Storage Temperature	T_{STG}	-55	150	℃	
Electrostatic Discharge (All Pins)	$V_{ESD(HBM)}$	1000		V	Human Body Model
	$V_{ESD(CDM)}$	1000		V	Charged Device Model

Notice

Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

Table 4 Recommended Operating Conditions

Parameter	Symbol	MIN	TYP	MAX	Unit
Operating Frequency	F_0	400		5000	MHz
RFFE Reference Voltage	V_{IO}	1.65	1.80	1.95	V
RFFE Bus Voltage (SDATA, SCLK) High	V_{IH}	0.8*VIO	VIO	VIO	V
RFFE Bus Voltage (SDATA, SCLK) Low	V_{IL}	0	0	0.2*VIO	V

Table 5 Nominal Operating Parameters

Parameter	Symbol	Specification MIN	TYP	MAX	Unit	Condition
Normal Conditions	V_{IO}=1.8V, V_{IH}=1.8V, V_{IL}=0V, P_{IN}=0dBm, VSWR=1:1, T_A=25℃, Unless Otherwise Stated					
DC Performances						
VIO Current	I_{IO}		300	350	μA	Active State
			40	45	μA	Low power State
RF Path Switching Time (One On Path to Another)	T_{SW}		1.5	2.0	μs	RF Switching CMD Implemented (50% SCLK) to 90%/10% RF Applied
Wake Up Time	T_{WP}		15	20	μs	Exiting Lower Power State CMD Implemented (50% SCLK) to 90% RF
Turn On Time	T_{ON}		15	20	μs	Cold Start, 50% VDD or VIO (the latter one to power up) to 90% RF
VIO Reset Time	T_{VIO_RST}	80			μs	VIO Reset Timing
RF Performances						
Insertion Loss (RFINx to RFOUTy)	IL		0.50	0.60	dB	F_0=400 to 960MHz
			0.63	0.70		F_0=1425 to 2200MHz
			0.65	0.80		F_0=2300 to 2690MHz
			0.90	1.10		F_0=3300 to 3800MHz
			1.50	1.70		F_0=3800 to 5000MHz
Isolation (Dual Through Mode, No-Adjacent Ports)	ISO	33	40		dB	F_0= 617 to 960MHz
		27	36			F_0= 1425 to 2200MHz
		26	34			F_0= 2300 to 2690MHz
		25	30			F_0= 3300 to 3800MHz
		23	28			F_0= 3800 to 5000MHz
Isolation (Dual Through Mode, Adjacent Ports)	ISO	23	27		dB	F_0= 617 to 960MHz
		17	23			F_0= 1425 to 2200MHz
		15	21			F_0= 2300 to 2690MHz
		13	16			F_0= 3300 to 3800MHz
		10	14			F_0= 3800 to 5000MHz
Input Return Loss (RFINx to RFOUTy)	RL	13	23		dB	F_0= 617 to 2200MHz
		10	15			F_0= 2300 to 5000MHz
Input 0.1dB Compression Point (RFINx to RFOUTy)	$P_{0.1dB}$		37		dBm	F_0= 617 to 960MHz, 20%DC
			36		dBm	F_0= 2300 to 2690MHz, 20%DC
			36		dBm	F_0= 3800 to 5000MHz, 20%DC

Parameter	Symbol	Specification MIN	TYP	MAX	Unit	Condition
2nd Order Harmonic	$2F_0$		-66	-63	dBm	F_0= 900MHz @26dBm
3rd Order Harmonic	$3F_0$		-85	-81	dBm	
2nd Order Harmonic	$2F_0$		-51	-49	dBm	F_0= 900MHz @35dBm
3rd Order Harmonic	$3F_0$		-64	-63	dBm	
2nd Order Harmonic	$2F_0$		-68	-67	dBm	F_0= 1800MHz @26dBm
3rd Order Harmonic	$3F_0$		-86	-85	dBm	
2nd Order Harmonic	$2F_0$		-54	-53	dBm	F_0= 1800MHz @33dBm
3rd Order Harmonic	$3F_0$		-63	-62	dBm	
2nd Order Harmonic	$2F_0$		-90	-83	dBm	F_0= 2600MHz @26dBm
3rd Order Harmonic	$3F_0$		-80	-78	dBm	
2nd Order Harmonic	$2F_0$		-81	-74	dBm	F_0= 2600MHz @30dBm
3rd Order Harmonic	$3F_0$		-68	-66	dBm	
2nd Order Harmonic	$2F_0$		-89	-81	dBm	F_0= 3500MHz @26dBm
3rd Order Harmonic	$3F_0$		-82	-80	dBm	
2nd Order Harmonic	$2F_0$		-81	-72	dBm	F_0= 3500MHz @30dBm
3rd Order Harmonic	$3F_0$		-70	-68	dBm	
2nd Order Harmonic	$2F_0$		-70	-69	dBm	F_0= 5000MHz @26dBm
3rd Order Harmonic	$3F_0$		-81	-79	dBm	
2nd Order Harmonic	$2F_0$		-63	-61	dBm	F_0= 5000MHz @30dBm
3rd Order Harmonic	$3F_0$		-70	-67	dBm	

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Tony.Wang@ChipSourceTek.com InFo@ChipSourceTek.com

MIPI RFFE Read and Write Timing

MIPI RFFE V2.1 protocol supports the following Command Sequences:

- Register Write
- Register Read
- Register_0 Write

Figure 3 and Figure 4 illustrate the timing diagrams for register write command sequence and read command sequence, respectively. Figure 5 describes the Register_0 write command sequence. In the below timing figures, SA[3:0] is the slave address. A[4:0] is the register address. D[7:0] is the data. “P” is a parity bit.

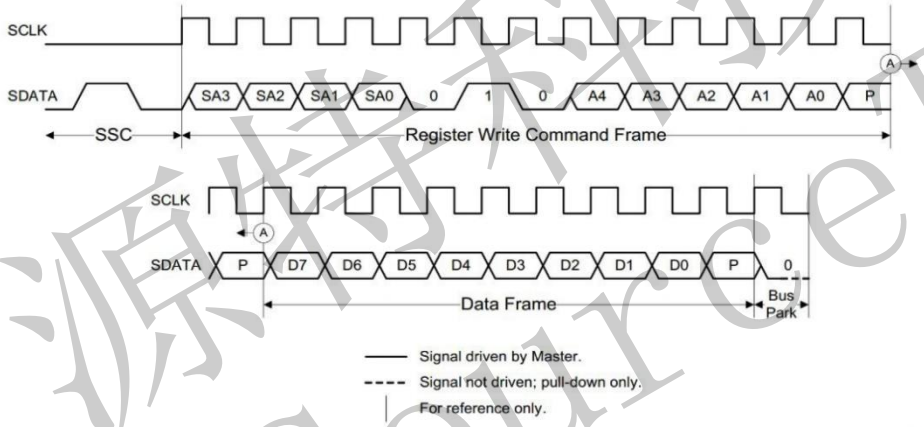


Figure 3 Register Write Command Sequence

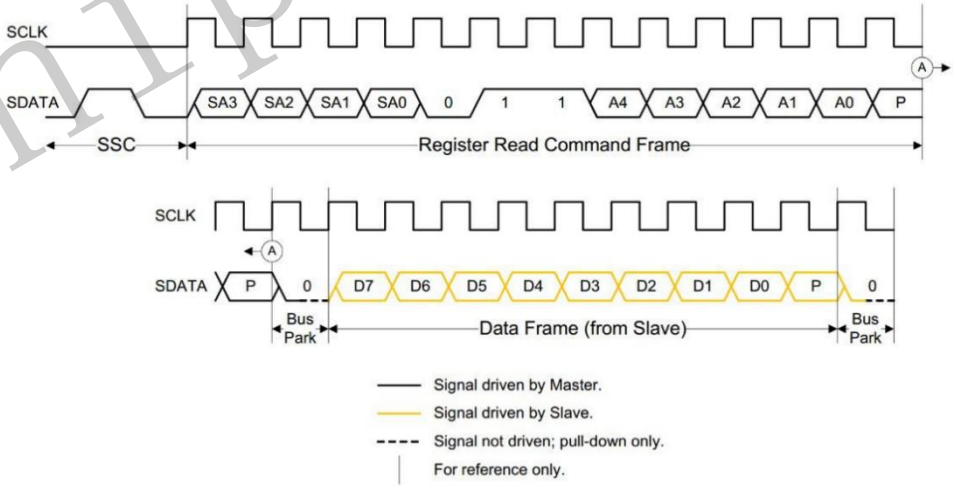


Figure 4 Register Read Command Sequence

Figure 5 shows the Register_0 Write Command Sequence. The Command Sequence starts with an SSC, followed by the Register 0 Write Command Frame containing the Slave address, a logic '1' (to denote the command type and address), and a only seven- bit word to be written into Register 0. The Command Sequence ends with a Bus Park Cycle.

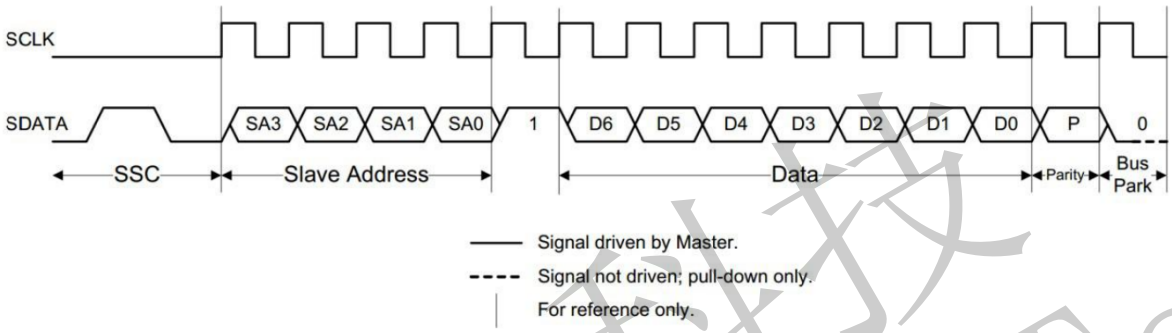


Figure 5 Register_0 Write Command Sequence

Other information such as MIPI USID programming sequence, MIPI bus specifications, etc. are stated in the MIPI Alliance Specification for RF Front-End Control Interface (RFFE), V2.1 (18-DEC-2017).

Register Definition

Table 6 Register Definition Table

Register Address	Register Name	Data Bits	R/W	Function	Description	Default	B/G ID	Trigger
0x00	REGISTER_0	7:0	R/W	RF Control 0	Register_0 Truth Table: Table 2	0x00	No	Yes
0x01	REGISTER_1	7:0	R/W	RF Control 1	Register_1 Truth Table: Table 2	0x00	No	Yes
0x1A	UDRST_ERR _SUM	7	R/W	SOFTWARE RESET	0b0: Normal operation 0b1: Software reset Note: During software reset, this register and all configurable registers are set to their default values except for reserved registers.	0b0	No	No
		6	R/W	COM_FP_P_ER	Command Frame with parity error	0b0	No	No
		5	R/W	COM_LEN_ER	Command Sequence with incorrect length	0b0	No	No
		4	R/W	ADD_FP_P_ER	Address Frame with parity error	0b0	No	No
		3	R/W	DAT_FP_P_ER	Data Frame with parity error	0b0	No	No
		2	R/W	RD_IVD_ADD	Read Command Sequence to an invalid address	0b0	No	No
		1	R/W	WR_IVD_ADD	Write Command Sequence to an invalid address	0b0	No	No
		0	R/W	BID_GID_ER	Read Command Sequence with a BSID or GSID Note: Reading this register resets this register.	0b0	No	No
0x1B	GROUP_SID	7:4	R	RESERVED	Reserved for future use	0x0	No	No
		3:0	R/W	GSID	Group Slave ID	0x0	No	No
		7	R/W	PWR_MODE_1	0b0: Normal Operation State Write Value:0b0, Read Value:0b0 0b1: Low	0b1	Yes	No

0x1C	PM_TRIG				Power State Write Value:0b1, Read Value:0b1			
		6	R/W	PWR_MODE_0	0b0: Normal Operation (Active) 0b1: Reset all registers to default settings (Startup) Write value: 0b1, Read Value: 0b0	0b0	Yes	No
					Note: Writing PWR_MODE_0 with a logic '1' will reset all register, and then automatically reenter the ACTIVE Mode.			
		5	R/W	Trigger_Mask_2	0b0: Trigger_2_Mask disabled 0b1: Trigger_2_ Mask enabled	0b0	No	No
		4	R/W	Trigger_Mask_1	0b0: Trigger_1_Mask disabled 0b1: Trigger_1_ Mask enabled	0b0	No	No
		3	R/W	Trigger_Mask_0	0b0: Trigger_0_Mask disabled 0b1: Trigger_0_ Mask enabled	0b0	No	No

Register Address	Register Name	Data Bits	R/W	Function	Description	Default	B/G ID	Trigger
		Note: If any one of the three Trigger Masks is set to a logic '1' the corresponding Trigger is disabled, in that case data written to a register associated with the Trigger goes directly to the destination register. Otherwise, if the Trigger Mask is enabled (via a logic '0'), incoming data is written to the shadow register, and the destination register is unchanged until its corresponding Trigger is asserted.						
		2	W	Trigger_2	0b0: Keep its associated destination registers unchanged 0b1:Load its associated destination registers with the data in the parallel shadow register, provided Trigger_Mask_2 is disabled(Logic '0')	0b0	Yes	No
		1	W	Trigger_1	0b0: Keep its associated destination registers unchanged 0b1:Load its associated destination registers with the data in the parallel shadow register, provided Trigger_Mask_1 is disabled(Logic '0')	0b0	Yes	No

		0	W	Trigger_0	0b0: Keep its associated destination registers unchanged 0b1:Load its associated destination registers with the data in the parallel shadow register, provided Trigger_Mask_0 is disabled(Logic '0')	0b0	Yes	No
0x1D	PRODUCT_ID	7:0	R	PRODUCT_ID	Product Number	0x1E	No	No
0x1E	MANUFACTURER_ID	7:0	R	MANUFACTURER_ID[7:0]	Lower eight bits of MIPI registered Manufacturer ID	0x78	No	No
0x1F	MAN_USID	7:4	R	MANUFACTURER_ID[11:8]	Upper four bits of MIPI registered Manufacturer ID	0x2	No	No
		3:0	R/W	USID	Unique Slave ID		No	No
					USID pin connected to VIO	0x6		
					USID pin connected to GND	0x7		

MIPI RFFE Operating Sequences

Here are some recommendations for MIPI RFFE operating sequences to prevent the device from damage.

1) Basic Operational Sequences

- Power On -- Apply Supply (VDD & VIO)-> Apply MIPI RFFE Bus (SCLK & SDATA) -> Apply RF Signal
- Power Off -- Remove RF Signal-> Remove MIPI RFFE Bus (SCLK & SDATA)->Remove Supply (VDD &VIO)

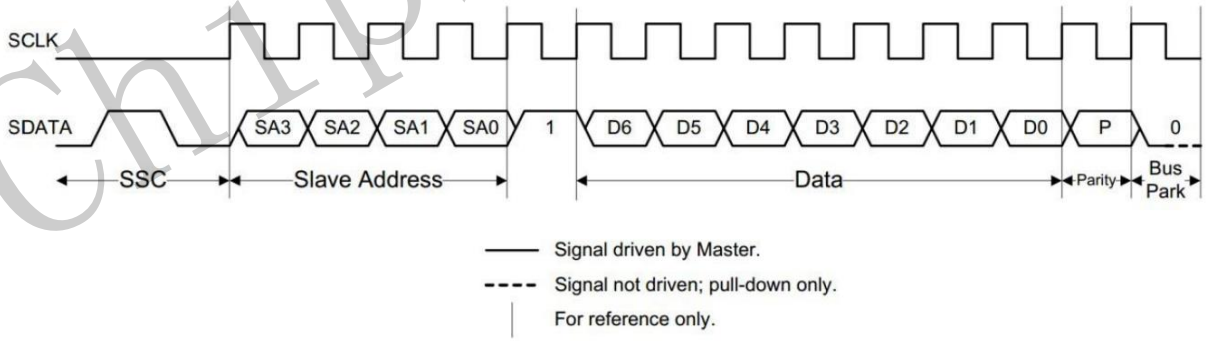


Figure 6 Basic Power On and Power Off Sequence

2) VDD and VIO may power on and off independently form one another. Besides, one power is allowed to powered off but to leave the other powered on if needed

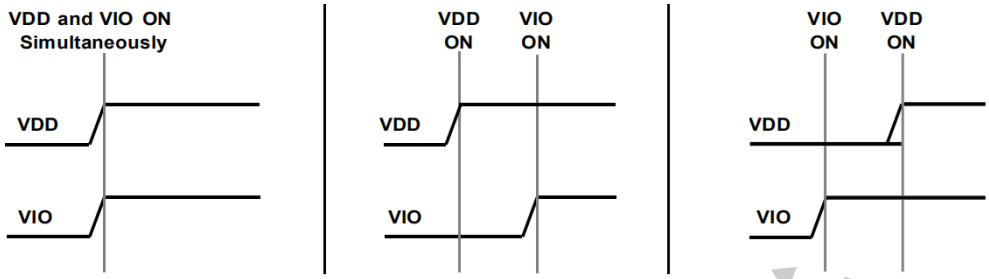


Figure 7 Allowed Power On Sequences

3) There shall be T_{ON}, after the latter supply powered on, before RF power is allowed to apply to any RF path.

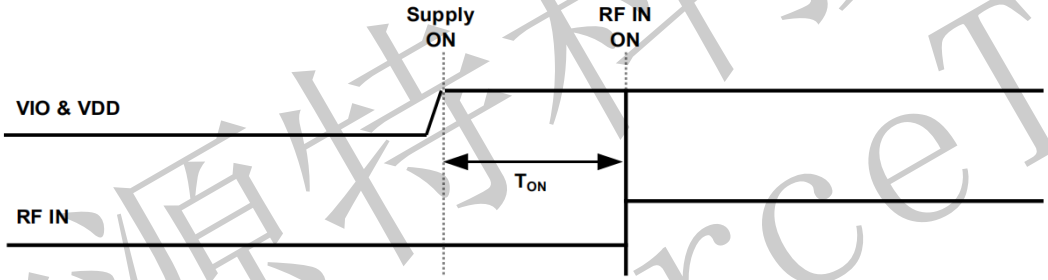


Figure 8 Supply and RF Signal On Sequence

4) To realize powered reset, after VIO enters the off state(VIO≤V_{VIO_RST}=200mV), it shall take VIO T_{VIO_RST}(≥10μs) to maintain the state before it is allowed to power up again. After then, VIO shall power up within T_{VIO_R}(≤400μs) to trigger POR.

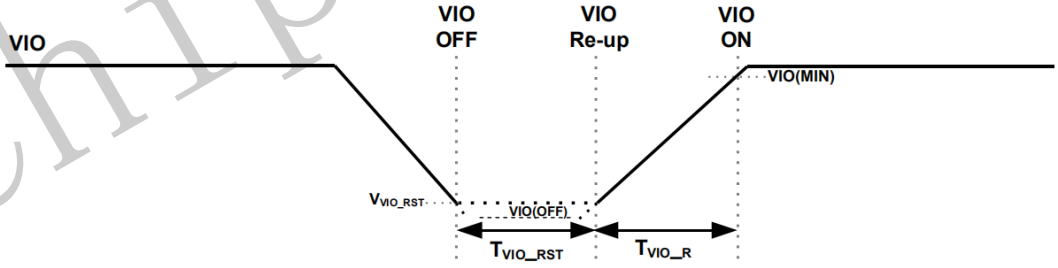


Figure 9 Powered Reset Sequence

5) To prevent the device from damage during switching events, RF signal shall be applied T_{SW} after the switching command is implemented and removed T_{SW} before any consequent switching command starts.

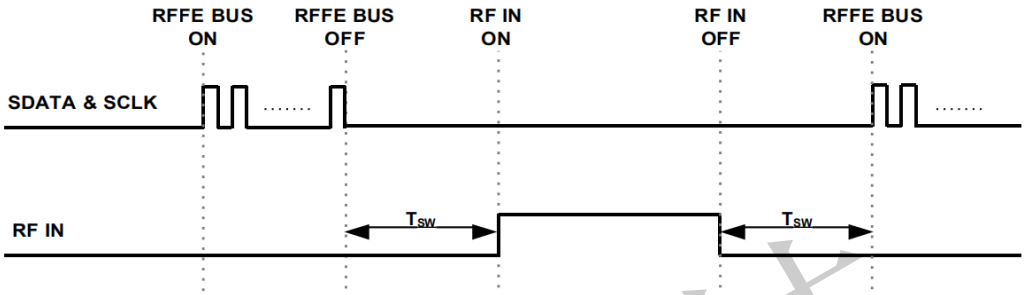


Figure 10 RF Power Switching Sequence

6) Large RF signal(>20dBm) shall not be applied during low power state. Hence, it shall be removed before the device enters low power state. After the device is switched from low power state to active state, there shall be at least T_{WK} before RF signal can be applied again.

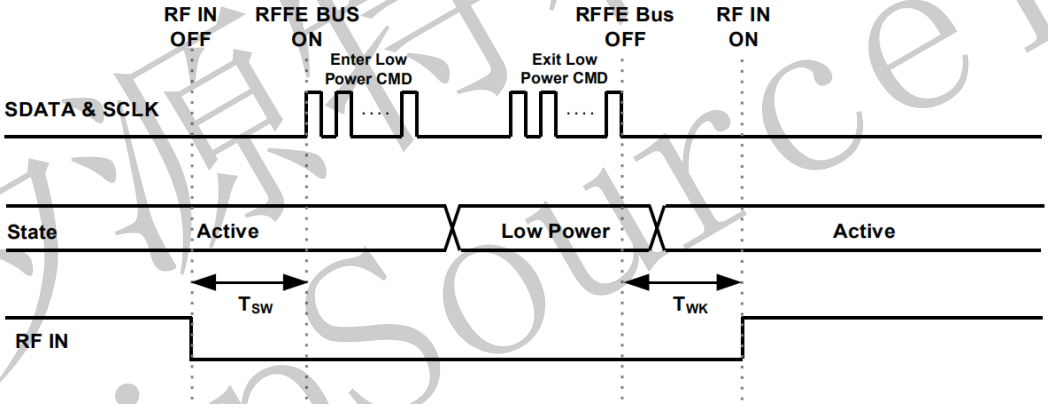
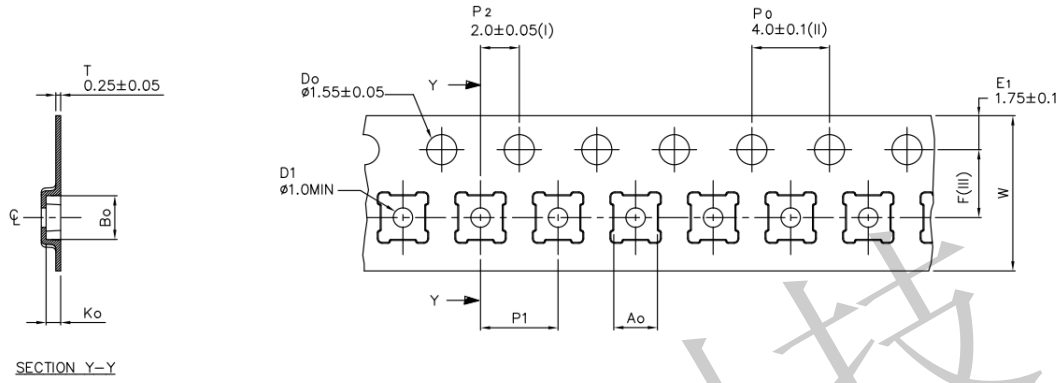


Figure 11 Enter and Exit Low Power State Sequence

Tape and Reel Dimensions



Ao	2.25 +/−0.1
Bo	2.25 +/−0.1
Ko	0.75 +/−0.1
F	3.50 +/−0.1
P1	4.00 +/−0.1
W	8.00 +/−0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Figure 12 Tape and Reel Dimensions

Reflow Chart

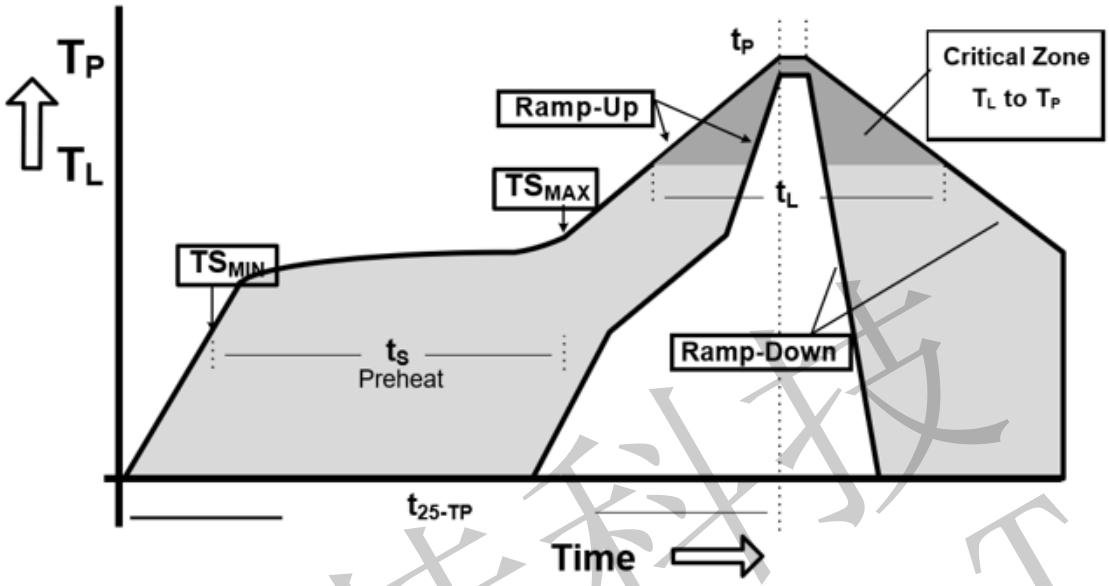


Figure 13 Recommended Lead-Free Reflow Profile

Table 7 Reflow Chart Parameters

Reflow Profile	Parameter
Preheat Temperature(TS_{MIN} to TS_{MAX})	150℃ to 200℃
Preheat Time(ts)	60 to 180 Seconds
Ramp-Up Rate(TS_{MAX} to T_P)	3℃/s MAX
Time Above T_L 217℃(t_L)	60 to 150 Seconds
Peak Temperature (T_P)	260℃
Time within 5℃ of Peak Temperature(t_P)	20 to 40 Seconds
Ramp-Down Rate(TS_{MAX} to T_P)	6℃/s MAX
Time for 25℃ to Peak Temperature(t_{25-TP})	8 Minutes MAX

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electric charge. Proper ESD protection techniques should be applied when devices are operated.

RoHS Compliant

This product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE), and are considered RoHS compliant.