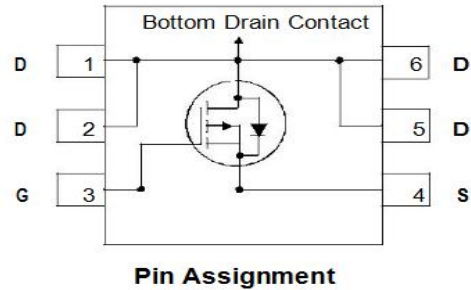




**P-Channel Enhancement Mode Power MOSFET**

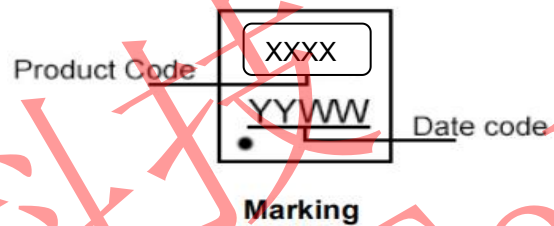
**Description**

The MXND805 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a load switching applications and a wide variety of other applications.



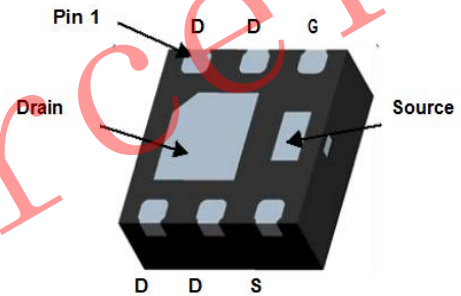
**General Features**

- ◆  $V_{DS} = -12V$ ,  $I_D = -8.5A$   
 @  $V_{GS} = -4.5V$   $R_{DS(ON)}(Typ.) = 14m\Omega$   
 @  $V_{GS} = -2.5V$   $R_{DS(ON)}(Typ.) = 19m\Omega$   
 @  $V_{GS} = -1.8V$   $R_{DS(ON)}(Typ.) = 29m\Omega$
- ◆ Advanced trench MOSFET process technology
- ◆ Ultra low on-resistance with low gate charge
- ◆ New Thermally Enhanced DFN2X2-6L Package



**Application**

- ◆ PWM applications
- ◆ Load switch
- ◆ battery charge in cellular handset



**DFN2x2-6L Pin definition and Top / Bottom View**

**Absolute Maximum Ratings (TA=25°C unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-12	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Drain Current-Continuous	$I_D$	-8.5	A
Drain Current-Pulsed (Note 1)	$I_{DM}$	-32	A
Maximum Power Dissipation	$P_D$	2.8	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	°C



**Electrical Characteristics** (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA	-12	-15	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-12V, V <sub>GS</sub> =0V	-	-	-1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±12V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>On Characteristics (Note 3)</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-0.4	-0.65	-1.0	V
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-6A	-	14	18	mΩ
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-5A	-	19	25	
		V <sub>GS</sub> =-1.8V, I <sub>D</sub> =-2.5A	-	29	45	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =-5V, I <sub>D</sub> =-8A	-	33	-	S
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =-1A	-	-	-1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	-3.5	A
<b>Dynamic Characteristics (Note4)</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-6V, V <sub>GS</sub> =0V, F=1.0MHz	-	1370	-	PF
Output Capacitance	C <sub>oss</sub>		-	350	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	258	-	PF
<b>Switching Characteristics (Note 4)</b>						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =-6V, R <sub>L</sub> =0.75Ω V <sub>GS</sub> =-4.5V, R <sub>GEN</sub> =3Ω	-	11	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	25	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	70	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	42	-	nS
Total Gate Charge	Q <sub>g</sub>		-	13	-	nC
Gate-Source Charge	Q <sub>gs</sub>		V <sub>DS</sub> =-6V, I <sub>D</sub> =-8A, V <sub>GS</sub> =-4.5V	-	2	-
Gate-Drain Charge	Q <sub>gd</sub>		-	3	-	nC

**Notes:**

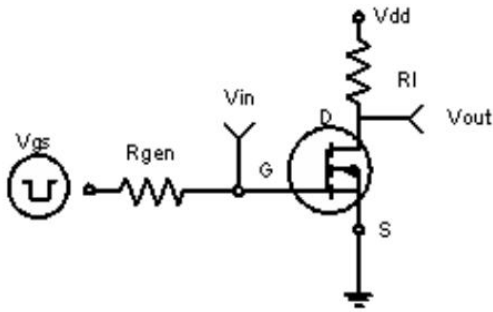
- surface mounted on FR4 board, t≤10sec
- pulse test: pulse width≤300μs, duty≤2%
- guaranteed by design, not subject to production testing

**Thermal Characteristics**

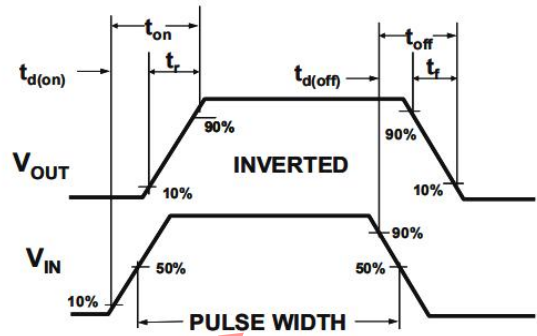
Thermal Resistance junction-to ambient	R <sub>th JA</sub>	45	°C/W
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### TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



Switching Test Circuit



Switching Waveforms

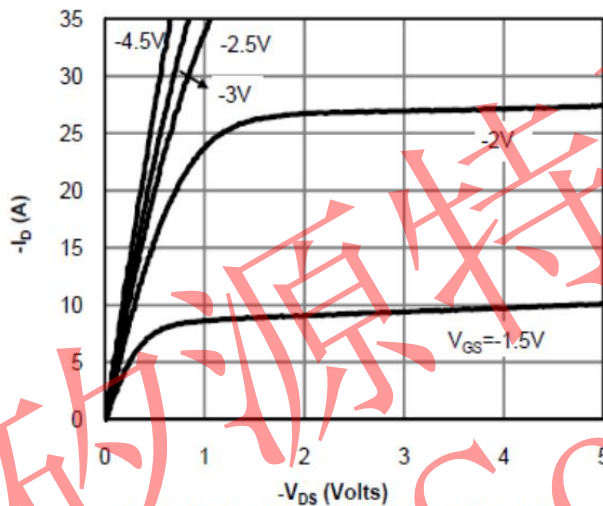


Fig 1: On-Region Characteristics (Note E)

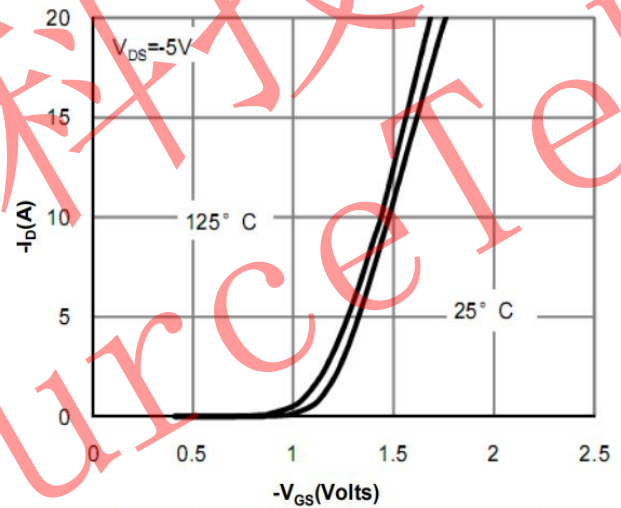


Figure 2: Transfer Characteristics (Note E)

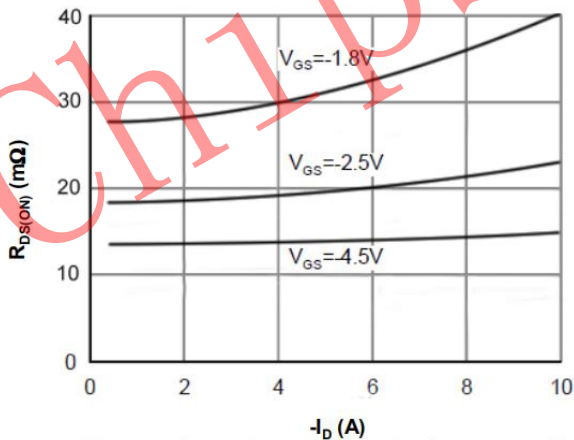


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

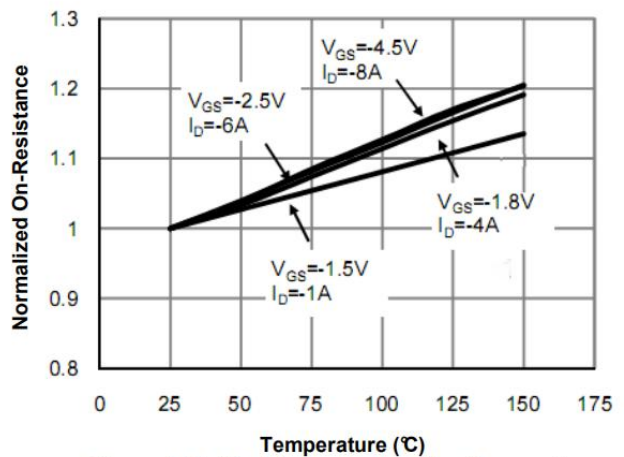


Figure 4: On-Resistance vs. Junction Temperature (Note E)

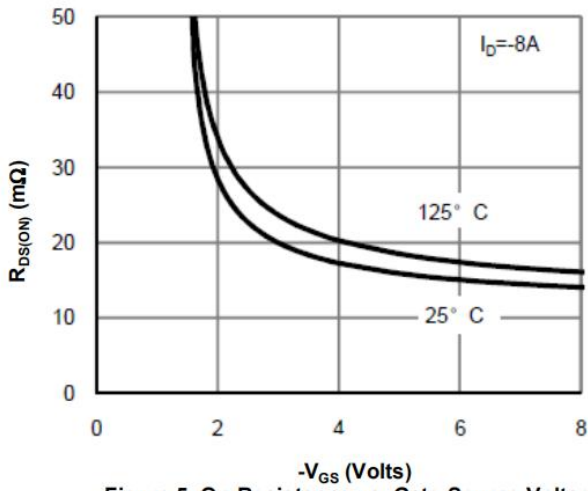


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

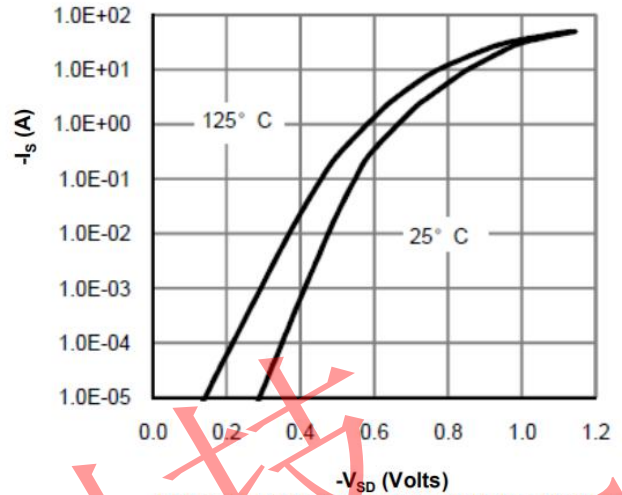


Figure 6: Body-Diode Characteristics (Note E)

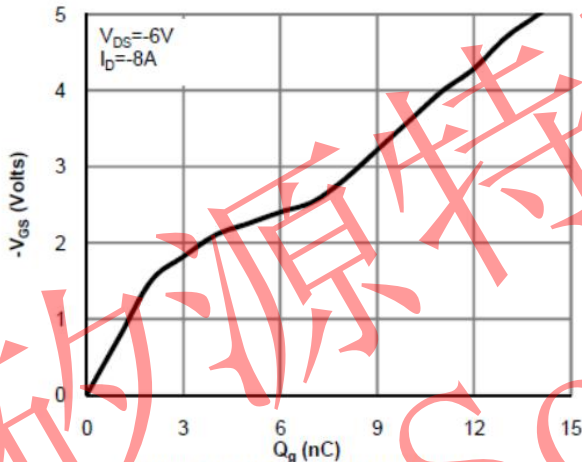


Figure 7: Gate-Charge Characteristics

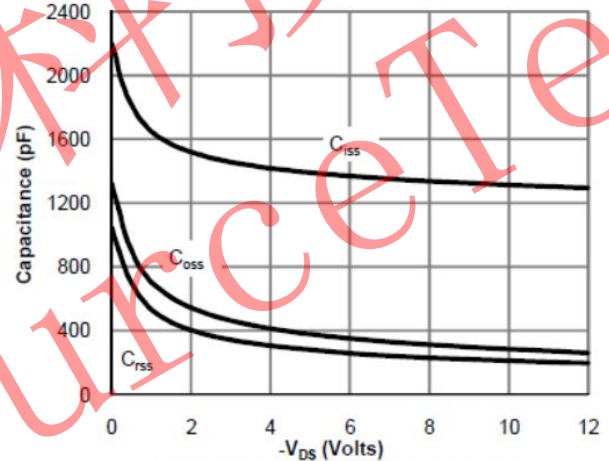


Figure 8: Capacitance Characteristics

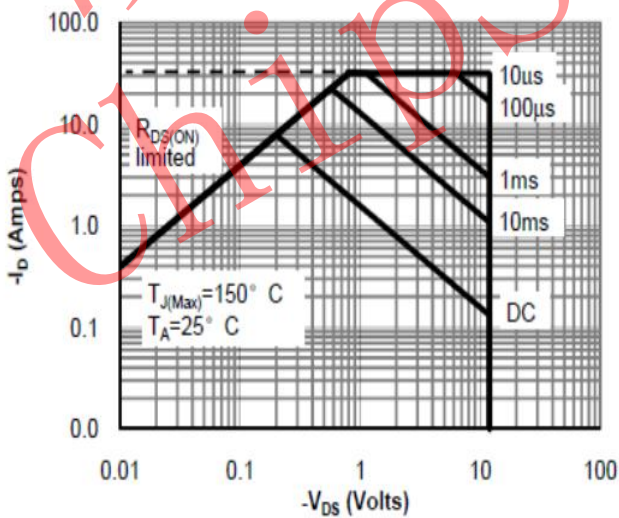


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

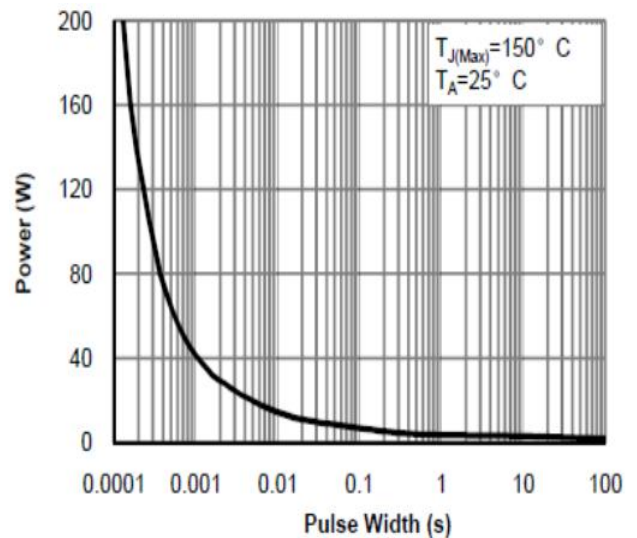
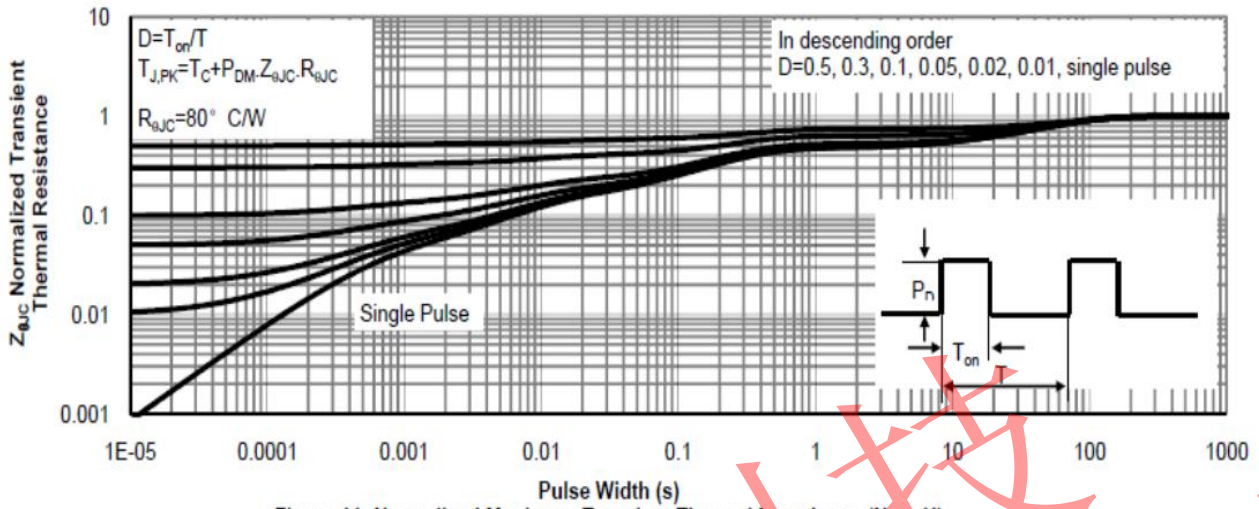


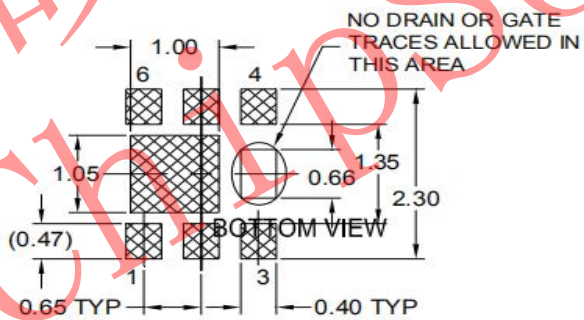
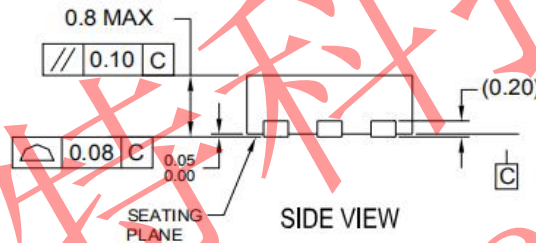
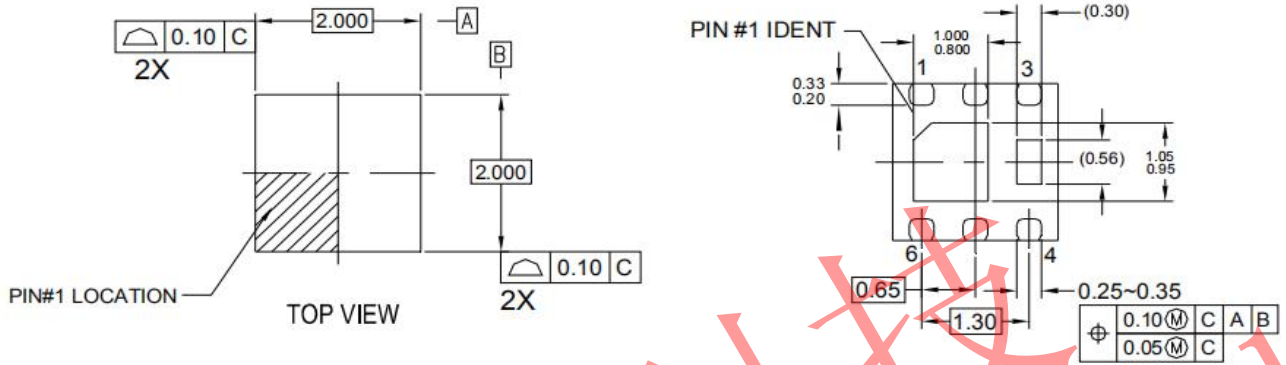
Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note H)



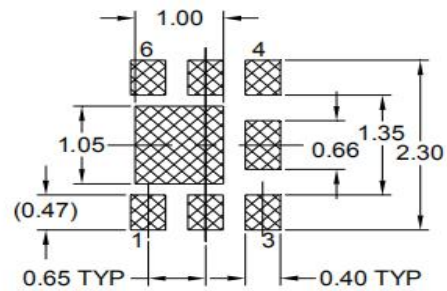
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DFN2x2-6L PACKAGE OUTLINE DIMENSIONS



RECOMMENDED LAND PATTERN OPT 1



RECOMMENDED LAND PATTERN OPT 2

**NOTES**

1. All dimensions are in millimeters.
2. Tolerance  $\pm 0.10\text{mm}$  (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.